REMARKS

Claims 1-18 are pending in the application. The Examiner notes that Figure 3 is informal. Claims 2-5, 9-12 and 16 are rejected under 35 U.S.C. §112, second paragraph. Claims 1, 2, 3, 4, 8, 9, 10, 11 and 15 are rejected under 35 U.S.C. §102(b). Claims 5, 6, 7, 12, 13, 14, 16, 17 and 18 are rejected under 35 U.S.C. §103(a). Applicants respectfully traverse these rejections for at least the reasons below and respectfully request the Examiner to reconsider and withdraw these rejections.

I. DRAWINGS:

The Examiner notes that Figure 3 is informal. Applicants will provide a formal Figure 3 upon allowance of claims 1-18.

II. REJECTIONS UNDER 35 U.S.C. §112:

The Examiner has rejected claims 2-5, 9-12 and 16 under 35 U.S.C. §112, second paragraph, for reciting the limitation of "minimal number of interface signals" without sufficient antecedent basis. Paper No. 3, page 2. Applicants kindly direct the Examiner's attention to the phrase "a minimal number of generic interface signals" in claims 1, 8 and 15. The phrase "a minimal number of generic interface signals" in claims 1, 8 and 15 provides sufficient antecedent basis for the limitation of "minimal number of interface signals" in claims 2, 9 and 16, respectively. Therefore, Applicants respectfully assert that claims 2-5, 9-12 and 16 are not properly rejected under 35 U.S.C. §112, second paragraph. Applicants respectfully request that the Examiner withdraw the rejections to claims 2-5, 9-12 and 16 under 35 U.S.C. §112, second paragraph.

III. REJECTIONS UNDER 35 U.S.C. §102(b):

The Examiner has rejected claims 1, 2, 3, 4, 8, 9, 10, 11 and 15 under 35 U.S.C. §102(b) as being anticipated by Mills. Paper No. 3, page 3. Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request that the Examiner reconsider and withdraw these rejections.

For a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. §2131.

Applicants respectfully assert that Mills does not disclose "providing transmit data path logic to receive and transmit data packets within the HPNA control chip" as recited in claim 1. The Examiner cites column 6, lines 16-21 of Mills as disclosing the above-cited claim limitation. Paper No. 3, page 3. Applicants respectfully traverse and assert that Mills instead discloses a line driver/receiver circuit that is coupled to communicate information with a font end multiplexer circuit. Column 6, lines 16-18. Mills further discloses that the select input of the front end multiplexer circuit is controlled by a control signal in a bus generated by an auto-negotiation circuit. Column 6, lines 18-21. There is no language in the cited passage that discloses an HPNA control chip. Applicants performed a search of the term "HPNA" and were unable to identify the term "HPNA" or any variation thereof. Further, there is no language within the cited passage that discloses providing transmit data path logic to receive data packets within a HPNA control chip. Neither is there any language within the cited passage that discloses providing transmit data path logic to transmit data packets within a HPNA control chip. Thus, Mills does not disclose all of the limitations of claim 1, and thus Mills does not anticipate claim 1. M.P.E.P. §2131.

Applicants further assert that Mills does not disclose "consolidating the transmit data path logic to include a transmit state machine that handles interfacing the transmit data path logic to at least two separate collision recovery logic means of the HPNA control chip through a minimal number of generic interface signals" as

recited in claim 1. As understood by the Applicants, the Examiner cites column 6, lines 16-21 and column 7, lines 1-5 of Mills as disclosing the above-cited claim limitation. Paper No. 3, page 3. Applicants respectfully traverse. As stated above, Mills instead discloses a line driver/receiver circuit that is coupled to communicate information with a font end multiplexer circuit. Column 6, lines 16-18. Mills further discloses that the select input of the front end multiplexer circuit is controlled by a control signal in a bus generated by an auto-negotiation circuit. Column 6, lines 18-21. Mills further discloses that the select input of the back end multiplexer is controlled by the control bus that receives part of its signal from the result of the auto-negation circuit and part of its signal from a management interface circuit. Column 7, lines 1-5. There is no language in the cited passage that discloses consolidating a transmit data path logic to include a transmit state machine. Applicants performed a search of the phrase "state machine" in Mills and were unable to identify the phrase "state machine" or any variation thereof in Mills. Neither is there any language in the cited passage that discloses consolidating a transmit data path logic to include a transmit state machine that handles interfacing the transmit data path logic to at least two separate collision recovery logic means. Neither is there any language in the cited passage that discloses consolidating a transmit data path logic to include a transmit state machine that handles interfacing the transmit data path logic to at least two separate collision recovery logic means of a HPNA control chip. Neither is there any language in the cited passage that discloses consolidating a transmit data path logic to include a transmit state machine that handles interfacing the transmit data path logic to at least two separate collision recovery logic means of a HPNA control chip through a minimal number of generic interface signals. Thus, Mills does not disclose all of the limitations of claim 1, and thus Mills does not anticipate claim 1. M.P.E.P. §2131.

Applicants further assert that Mills does not disclose "at least two collision recovery means for providing collision recovery in the HPNA control chip according to at least two data rate standards" as recited in claim 8. The Examiner has not cited to any passage in Mills as teaching the above-cited claim limitation. The Examiner is

reminded that in order to establish a *prima facie* case of anticipation, the Examiner must provide a single prior art reference that expressly or inherently describes each and every element as set forth in the claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631; M.P.E.P. §2131. Since the Examiner has not provided such evidence, the Examiner has not presented a *prima facie* case of anticipation in rejecting claim 8. M.P.E.P. §2131.

Applicants further assert that Mills does not disclose "a physical layer (PHY)" as recited in claim 15. The Examiner has not cited to any passage in Mills as teaching the above-cited claim limitation. The Examiner is reminded that in order to establish a *prima facie* case of anticipation, the Examiner must provide a single prior art reference that expressly or inherently describes each and every element as set forth in the claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631; M.P.E.P. §2131. Since the Examiner has not provided such evidence, the Examiner has not presented a *prima facie* case of anticipation in rejecting claim 15. M.P.E.P. §2131.

Applicants further assert that Mills does not disclose "a media access controller (MAC) coupled between the MII and the PHY" as recited in claim 15. The Examiner cites column 6, lines 16-21 and column 7, lines 1-5 of Mills as disclosing the above-cited claim limitation. Paper No. 3, page 4. Applicants respectfully traverse. As stated above, Mills instead discloses a line driver/receiver circuit that is coupled to communicate information with a font end multiplexer circuit. Column 6, lines 16-18. Mills further discloses that the select input of the front end multiplexer circuit is controlled by a control signal in a bus generated by an auto-negotiation circuit. Column 6, lines 18-21. Mills further discloses that the select input of the back end multiplexer is controlled by the control bus that receives part of its signal from the result of the auto-negation circuit and part of its signal from a management interface circuit. Column 7, lines 1-5. There is no language in the cited passage that discloses a media access controller. Neither is there any language in the cited passage that discloses a media access controller coupled between a media independent

interface and a physical layer. Thus, Mills does not disclose all of the limitations of claim 15, and thus Mills does not anticipate claim 15. M.P.E.P. §2131.

Applicants further assert that Mills does not disclose "the MAC further comprising at least two collision recovery means for providing collision recovery according to at least to two data rate standards, and a transmit data path logic means including a transmit state machine that interfaces with at least two collision recovery means through a minimal number of generic interface signals" as recited in claim 15. As understood by the Applicants, the Examiner cites column 6, lines 60-65 and column 7, lines 61-65 of Mills as disclosing the above-cited claim limitation. Paper No. 3, page 4. Applicants respectfully traverse and assert that Mills instead discloses that MII one circuit is for communicating with a first collision domain and MII two circuit is for communicating with a second collision domain. Column 6, lines 60-63. Mills further discloses that the switching functionality of the physical device can be controlled by the auto-negation circuit providing seamless switching between 100 M and 10 M domains without external switching circuitry. Column 7, lines 61-65. There is no language in the cited passages that discloses two collision recovery means for providing collision recovery according to at least to two data rate standards. Neither is there any language in the cited passages that discloses a transmit data path logic means that includes a transmit state machine. Neither is there any language in the cited passages that discloses a transmit data path logic means that includes a transmit state machine that interfaces with at least two collision recovery means. Neither is there any language in the cited passages that discloses a transmit data path logic means that includes a transmit state machine that interfaces with at least two collision recovery means through a minimal number of generic interface signals. Thus, Mills does not disclose all of the limitations of claim 15, and thus Mills does not anticipate claim 15. M.P.E.P. §2131.

Further, in connection with the rejection to the above-cited claim limitation, the Examiner asserts that a first collision domain and a second collision domain, as disclosed in Mills, is the same as providing collision recovery according to at least to

two data rate standards. Paper No. 3, page 4. Applicants respectfully traverse. The Examiner must provide a basis in fact and/or technical reasoning to support the assertion that a first collision domain and a second collision domain, as disclosed in Mills, is the same as providing collision recovery according to at least to two data rate standards. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that a first collision domain and a second collision domain, as disclosed in Mills, is the same as providing collision recovery according to at least to two data rate standards, and that it be so recognized for persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745, 49 U.S.P.Q.2d 1949, 1950-51 (Fed. Cir. 1999). Since the Examiner has not provided such evidence, the Examiner has not presented a *prima facie* case of anticipation in rejecting claim 15. M.P.E.P. § 2131.

Claims 2-4 recite the combinations of claim 1 and thus are not anticipated for at least the above-stated reasons as to why claim 1 is not anticipated by Mills. Further, claims 9-11 recite the combinations of claim 8 and thus are not anticipated for at least the above-stated reasons as to why claim 8 is not anticipated by Mills. Claims 2-4 and 9-11 recite additional features, which, in combination with the features of the claims upon which they depend are not anticipated by Mills.

For example, Mills does not disclose "wherein the minimal number of interface signals further comprises a GO signal from each separate collision recovery logic means" as recited in claim 2 and similarly in claim 9. The Examiner cites column 7, lines 61-65 of Mills as disclosing the above-cited claim limitation. Paper No. 3, page 3. Applicants respectfully traverse and assert that Mills instead discloses that the switching functionality of the physical device can be controlled by the auto-negation circuit providing seamless switching between 100 M and 10 M domains without external switching circuitry. Column 7, lines 61-65. There is no language in the cited passage that discloses that a minimal number of interface signals includes a GO signal. Neither is there any language in the cited passage that discloses that a minimal number of interface signals includes a GO signal from each separate

collision recovery logic means. Thus, Mills does not disclose all of the limitations of claims 2 and 9, and thus Mills does not anticipate claims 2 and 9. M.P.E.P. §2131.

Applicants further assert that Mills does not disclose "wherein the minimal number of interface signals further comprises a new transmit signal" as recited in claim 3 and similarly in claim 10. The Examiner cites column 7, lines 61-65 of Mills as disclosing the above-cited claim limitation. Paper No. 3, page 3. Applicants respectfully traverse and assert that Mills instead discloses that the switching functionality of the physical device can be controlled by the auto-negation circuit providing seamless switching between 100 M and 10 M domains without external switching circuitry. Column 7, lines 61-65. There is no language in the cited passage that discloses that a minimal number of interface signals includes a new transmit signal. Thus, Mills does not disclose all of the limitations of claims 3 and 10, and thus Mills does not anticipate claims 3 and 10. M.P.E.P. §2131.

Applicants further assert that Mills does not disclose "wherein the minimal number of interface signals further comprises a transmit done signal" as recited in claim 4 and similarly in claim 11. The Examiner cites column 7, lines 61-65 of Mills as disclosing the above-cited claim limitation. Paper No. 3, page 4. Applicants respectfully traverse and assert that Mills instead discloses that the switching functionality of the physical device can be controlled by the auto-negation circuit providing seamless switching between 100 M and 10 M domains without external switching circuitry. Column 7, lines 61-65. There is no language in the cited passage that discloses that a minimal number of interface signals includes a transmit done signal. Thus, Mills does not disclose all of the limitations of claims 4 and 11, and thus Mills does not anticipate claims 4 and 11. M.P.E.P. §2131.

As a result of the foregoing, Applicants respectfully assert that not each and every claim limitation was found within Mills, and thus claims 1-4, 8-11 and 15 are not anticipated by Mills.

III. REJECTIONS UNDER 35 U.S.C. §103(a):

The Examiner has rejected claims 5-7, 12-14 and 16-18 under 35 U.S.C. § 103(a) as being unpatentable over Mills in view of Lu et al. (U.S. Patent No. 6,839,345) (hereinafter "Lu"). Paper No. 3, page 5. Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request that the Examiner reconsider and withdraw these rejections.

A. The Examiner has not provided any objective evidence or appropriate motivation for modifying Mills with Lu.

A *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. §2142. The showings must be clear and particular and supported by objective evidence. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

The Examiner admits that Mills does not teach the limitation of claims 5 and 12 ("wherein the minimal number of interface signals further comprises a transmit priority indicator from the transmit data"). Paper No. 3, page 5. The Examiner further admits that Mills does not teach "wherein the minimal number of interface signals further comprises....a transmit priority indicator from the transmit data" as recited in claim 16. Paper No. 3, page 5. The Examiner's motivation for modifying Mills with Lu to incorporate the above-cited claim limitations is "so as to provide a QOS guarantee at the physical layer (Lu, column 2, lines 17-29)." Paper No. 3, page 5. The Examiner's motivation is insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

The Examiner's motivation does not address as to why one of ordinary skill in the art with the primary reference (Mills) in front of him would modify Mills to have a minimal number of interface signals include a transmit priority indicator from the transmit data in light of the teachings of the secondary reference (Lu). Mills teaches a multi-communication rate switching physical device for recovering bits from a wire connection that is coupled to a computer system adapter. Abstract. The Examiner's motivation of "to provide a QOS guarantee at the physical layer" does not address as to why one of ordinary skill in the art would modify Mills, which teaches a multi-communication rate switching physical device for recovering bits from a wire connection that is coupled to a computer system adapter, to have a minimal number of interface signals include a transmit priority indicator from the transmit data. The Examiner is merely relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 5,12 and 16. *Id.*

Further, the Examiner admits that Mills does not teach the limitation of claims 6, 13 and 17 ("wherein the at least two separate collision recovery logic means further comprises a BEB collision recovery means"). Paper No. 3, page 6. The Examiner's motivation for modifying Mills with Lu to incorporate the above-cited claim limitations is "to defer its transmission when media is busy (Lu, column 2, lines 12-17)." Paper No. 3, page 6. The Examiner's motivation is insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

The Examiner's motivation does not address as to why one of ordinary skill in the art with the primary reference (Mills) in front of him would modify Mills to have two separate collision recovery logic means include a BEB collision recovery means. Mills teaches a multi-communication rate switching physical device for recovering bits from a wire connection that is coupled to a computer system adapter. Abstract. The Examiner cites column 2, lines 12-17 of Lu as support for this motivation to modify Mills to include the above-cited claim limitation. Paper No. 3, page 6. Lu

teaches that the Ethernet MAC uses a binary exponential backoff algorithm to defer its transmission when media is busy. Column 2, lines 12-17. The Examiner's motivation of having a MAC using a binary exponential backoff algorithm to defer its transmission when the media is busy does not address as to why one of ordinary skill in the art would modify Mills, which teaches a multi-communication rate switching physical device for recovering bits from a wire connection that is coupled to a computer system adapter, to have at least two separate collision recovery logic means include a BEB collision recovery means. The passage that the Examiner cited in Lu to support his motivation teaches a MAC that uses a binary exponential backoff algorithm to defer its transmission when the media is busy. The Examiner is merely relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 6, 13 and 17. *Id.*

B. The Examiner has not provided any motivation for modifying Mills with Lu to incorporate the limitations of claims 7, 14 and 18.

The Examiner admits that Mills does not teach the limitation of claims 7, 14 and 18 ("wherein the at least two separate collision recovery logic means further comprises a DFPQ collision recovery means"). Paper No. 3, page 6. The Examiner has not provided any motivation for modifying Mills with Lu to include the above-cited claim limitation. The Examiner must provide a motivation for modifying Mills with Lu to include the above-cited claim limitation in order to establish a *prima facie* case of obviousness. M.P.E.P. §2143. Since the Examiner has not provided such a motivation, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 7, 14 and 18. *Id.*

C. Mills and Lu, taken singly or in combination, do not teach or suggest the following claim limitations.

Applicants respectfully assert that Mills and Lu, taken singly or in combination, do not teach or suggest "wherein the minimal number of interface

signals further comprises a transmit priority indicator from the transmit data" as recited in claim 5 and similarly in claim 12. The Examiner cites column 4, lines 52-56 of Lu as teaching the above-cited claim limitation. Paper No. 3, page 5. Applicants respectfully traverse and assert Lu instead teaches that in the home networking area, the Deference Algorithm module implements BEB on HPNA 1.0 or Ethernet 802.3 MAC, DFPQ on HPNA 2.0 and CSMA/CA and NAV on 802.11 MAC implementations. Column 4, lines 52-56. There is no language in the cited passage that teaches that a minimal number of interface signals includes a transmit priority indicator from the transmit data. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 5 and 12, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Applicants further assert that Mills and Lu, taken singly or in combination, do not teach or suggest "wherein the minimal number of interface signals further comprises a GO signal from each collision recovery means, a new transmit signal, a transmit done signal and a transmit priority indicator from the transmit data" as recited in claim 16. The Examiner cites column 7, lines 61-65 of Mills as teaching all of the above-cited claim limitations except "transmit priority indicator from the transmit data." Paper No. 3, page 5. The Examiner further cites column 4, lines 52-56 of Lu as teaching the claim limitation of "transmit priority indicator from the transmit data." Paper No. 3, page 5. Applicants respectfully traverse.

As stated above, Mills instead teaches that the switching functionality of the physical device can be controlled by the auto-negation circuit providing seamless switching between 100 M and 10 M domains without external switching circuitry. Column 7, lines 61-65. There is no language in the cited passage that teaches that a minimal number of interface signals includes a GO signal. Neither is there any language in the cited passage that teaches that a minimal number of interface signals includes a GO signal from each separate collision recovery logic means. Neither is there any language in the cited passage that teaches that a minimal number of

interface signals includes a new transmit signal. Neither is there any language in the cited passage that teaches that a minimal number of interface signals includes a transmit done signal. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 16, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Furthermore, as stated above, Lu instead teaches that in the home networking area, the Deference Algorithm module implements BEB on HPNA 1.0 or Ethernet 802.3 MAC, DFPQ on HPNA 2.0 and CSMA/CA and NAV on 802.11 MAC implementations. Column 4, lines 52-56. There is no language in the cited passage that teaches that a minimal number of interface signals includes a transmit priority indicator from the transmit data. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 16, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Applicants further assert that Mills and Lu, taken singly or in combination, do not teach or suggest "wherein the at least two separate collision recovery logic means further comprises a BEB collision recovery means" as recited in claim 6 and similarly in claims 13 and 17. The Examiner asserts that Mills teaches two separate collision recovery means. Paper No. 3, page 6. For at least the reasons stated above, Mills does not teach or suggest two separate collision recovery means. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 6, 13 and 17, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Applicants further assert that Mills and Lu, taken singly or in combination, do not teach or suggest "wherein the at least two separate collision recovery logic means further comprises a DFPQ collision recovery means" as recited in claim 7 and similarly in claims 14 and 18. The Examiner cites column 4, lines 52-56 of Lu as teaching the above-cited claim limitation. Paper No. 3, page 6. Applicants

respectfully traverse and assert that Lu instead teaches that the deference algorithm modules implements DFPQ on HPNA 2.0. Column 4, lines 52-55. There is no language in the cited passage that teaches two separate collision recovery logic means. Neither is there any language in the cited passage that teaches two separate collision recovery logic means that includes a DFPQ collision recovery means. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 7, 14 and 18, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

D. The Examiner has not presented a reasonable expectation of success when combining Mills with Lu.

The Examiner must present a reasonable expectation of success in combining Mills with Lu in order to establish a *prima facie* case of obviousness. M.P.E.P. §2143.02.

Mills teaches a multi-communication rate switching physical device for a port of a mixed communication rate Ethernet repeater network. Abstract. Mills further teaches a physical device for recovering bits from a wire connection that is coupled to a computer system adapter. Abstract. Mills further teaches that the physical device can be implemented on a single chip integrated within an Ethernet repeater hub within each hub port. Abstract.

Lu, on the other hand, teaches managing data flow over an open system interconnection type network which includes a physical layer and a media access control layer. Abstract.

The Examiner has not presented any evidence that there would be a reasonable expectation of success in combining Mills, which teaches a multi-communication rate switching physical device for recovering bits from a wire connection that is coupled to a computer system adapter, with Lu, which teaches managing data flow over an open system interconnection type network which

includes a physical layer and a media access control layer. The Examiner must provide objective evidence as to how a multi-communication rate switching physical device for recovering bits from a wire connection can be combined with a system that manages data flow over an open system interconnection type network. M.P.E.P. §2143.02. Since the Examiner has not provided such evidence, the Examiner has not presented a reasonable expectation of success in combining Mills with Lu. M.P.E.P. §2143.02. Accordingly, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 5-7, 12-14 and 16-18. M.P.E.P. §2143.02.

IV. CONCLUSION

As a result of the foregoing, it is asserted by Applicants that claims 1-18 in the Application are in condition for allowance, and Applicants respectfully request an allowance of such claims. Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining issues.

Respectfully submitted,

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